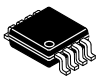
P2040B

Product Preview

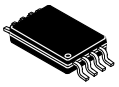
LCD Panel EMI Reduction IC

ON Semiconductor®

http://onsemi.com

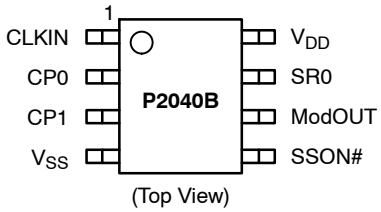


SOIC−8
S SUFFIX
CASE 751BD



TSSOP−8
T SUFFIX
CASE 948AL

PIN CONFIGURATION



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

Description

The P2040B is a selectable spread spectrum frequency modulator designed specifically for digital flat panel applications. The P2040B reduces electromagnetic interference (EMI) at the clock source which provides system wide reduction of EMI of all clock dependent signals.

The P2040B allows significant system cost savings by reducing the number of circuit board layers and shielding that are traditionally required to pass EMI regulations.

The P2040B uses the most efficient and optimized modulation profile approved by the FCC and is implemented in a proprietary all digital method.

The P2040B modulates the output of a single PLL in order to "spread" the bandwidth of a synthesized clock and, more importantly, decreases the peak amplitudes of its harmonics.

This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal's bandwidth is called 'spread spectrum clock generation.'

Applications

The P2040B is targeted towards digital flat panel applications for Notebook PCs, Palm−size PCs, Office Automation Equipments, and LCD Monitors.

Features

- Provides up to 15 dB of EMI Suppression
- FCC Approved Method of EMI Attenuation
- Generates a Low EMI Spread Spectrum Clock of the Input Frequency
- 30 MHz to 100 MHz Input Frequency Range
- Optimized for 32.5 MHz, 54 MHz, 65 MHz, 81 MHz, Pixel Clock Frequencies
- Internal Loop Filter Minimizes External Components and Board Space
- 8 Selectable Spread Ranges, up to ±2.0%
- SSON# Control Pin for Spread Spectrum Enable and Disable Options
- Low Cycle−to−Cycle Jitter
- 3.3 V Operating Voltage
- Ultra Low Power CMOS Design
- Supports Most Mobile Graphic Accelerator and LCD Timing Controller Specifications
- Available in 8−pin SOIC and TSSOP Packages
- These are Pb−Free Devices

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

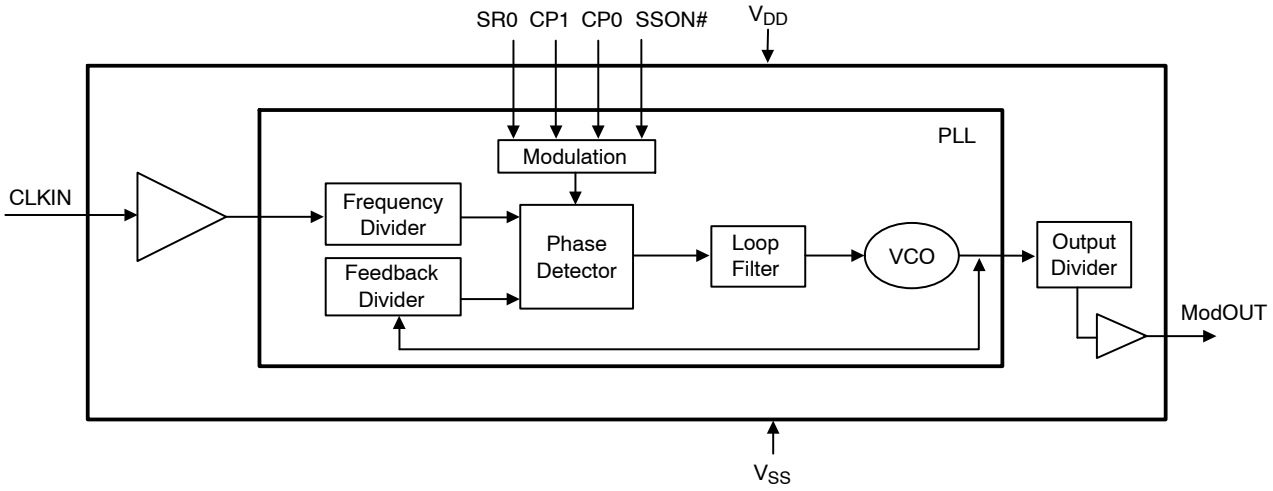


Figure 1. Block Diagram

Table 1. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to Ground	−0.5 to +4.6	V
T_{STG}	Storage temperature	−65 to +125	°C
T_A	Operating temperature	−40 to +85	°C
T_s	Max. Soldering Temperature (10 sec)	260	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22− A114−B)	2	KV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 2. DEVIATIONS AND MODULATION RATE TABLE

			Spreading Range (±%)				
CP0	CP1	SR0	32.5 MHz	54 MHz	65 MHz	81 MHz	Modulation Rate
0	0	0	0.56	1.05	1.00	0.98	(Fin/40) * 62.49 KHz
0	0	1	1.94	1.68	1.56	1.48	(Fin/40) * 62.49 KHz
0	1	0	1.36	1.05	1.00	0.92	(Fin/40) * 62.49 KHz
0	1	1	1.92	1.68	1.56	1.48	(Fin/40) * 62.49 KHz
1	0	0	1.24	0.81	0.66	0.40	(Fin/40) * 62.49 KHz
1	0	1	1.91	1.29	1.02	0.74	(Fin/40) * 62.49 KHz
1	1	0	0.91	0.45	0.34	0.05	(Fin/40) * 62.49 KHz
1	1	1	1.47	0.71	0.54	0.36	(Fin/40) * 62.49 KHz

Table 3. PIN DESCRIPTION

Pin#	Pin Name	Type	Description
1	CLKIN	I	External reference frequency input. Connect to externally generated reference signal.
2	CP0	I	Digital logic input used to select charge pump current (see Table 2). This pin has a 100 KΩ internal pull−up resistor.
3	CP1	I	Digital logic input used to select charge pump current (see Table 2). This pin has a 100 KΩ internal pull−up resistor.
4	V_{SS}	P	Ground Connection. Connect to system ground.
5	SSON#	I	Digital logic input used to enable Spread Spectrum function (Active LOW). Spread Spectrum function enable when LOW. This pin has a 100 KΩ internal pull−low resistor.
6	ModOUT	O	Spectrum Clock output.
7	SR0	I	Digital logic input used to select Spreading Range (see Table 2). This pin has a 100 KΩ internal pull−up resistor.
8	V_{DD}	P	Connect to +3.3 V.

Table 4. DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter		Min	Typ	Max	Unit
V_{IL}	Input Low voltage		V_{SS}−0.3	–	0.8	V
V_{IH}	Input High voltage		2.0	–	V_{DD}+0.3	V
I_{IL}	Input Low current (100 KΩ input pull−up resistor on inputs SR0, CP1 and CP0)		–	–	−35	μA
I_{IH}	Input High current (100 KΩ input pull−low resistor on input SSON#)		–	–	35	μA
V_{OL}	Output Low current	V_{DD} = 3.3 V, I_{OL} = 20 mA	–	–	0.4	V
V_{OH}	Output High current	V_{DD} = 3.3 V, I_{OH} = 20 mA	2.5	–	–	V
I_{DD}	Static Supply Current		–	0.6	–	mA
I_{CC}	Dynamic Supply Current (3.3 V and 15 pF loading)		9	16	22	mA
V_{DD}	Operating Voltage		3.0	3.3	3.6	V
t_{ON}	Power up time (first locked clock cycle after power up)		–	0.18	–	mS
Z_{OUT}	Clock Output impedance		–	50	–	Ω

Table 5. AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter		Min	Typ	Max	Unit
f_{IN}	Input Frequency		30	–	100	MHz
f_{OUT}	Output Frequency		30	–	100	MHz
t_{LH} (Note 1)	Output Rise time	Measured at 0.8 V to 2.0 V	0.7	0.9	1.1	nS
t_{HL} (Note 1)	Output Fall time	Measured at 2.0 V to 0.8 V	0.6	0.8	1.0	nS
t_{JC}	Jitter (cycle−to−cycle)		–	360	–	pS
t_D	Output Duty cycle		45	50	55	%

1. t_{LH} and t_{HL} are measured into a capacitive load of 15 pF.

Spread Spectrum Selection

Table 2 illustrates the possible spread spectrum options. The optimal setting should minimize system EMI to the fullest without affecting system performance. The spreading is described as a percentage deviation of the center frequency (Note: the center frequency is the frequency of the external reference input on CLKIN, Pin 1).

Example:

P2040B is designed for high resolution flat panel applications and is able to support panel frequencies from 30 MHz to 100 MHz. For a 65 MHz pixel clock frequency, a spreading selection of CP0 = 0, CP1 = 1 and SR0 = 1 gives a percentage deviation of ±1.56% (see Table 2). This results in frequency on ModOUT being swept from 64.5 MHz to 65.5 MHz. This particular example given here is a common EMI reduction method for notebook LCD panel and has already been implemented by most of the leading OEM and mobile graphic accelerator manufacturers.

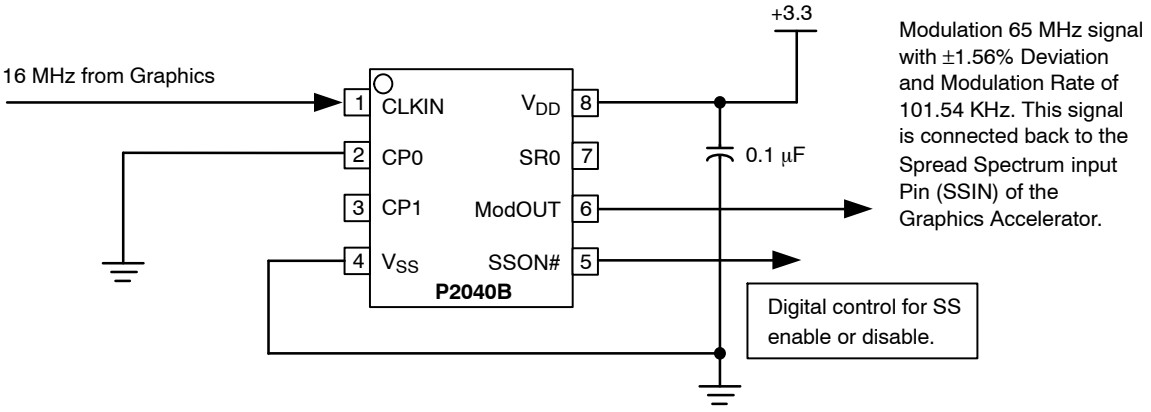
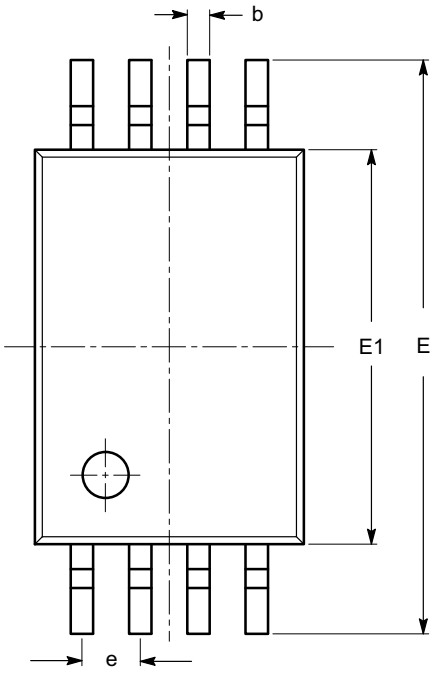


Figure 2. Application Schematic for Mobile LCD Graphics Controllers

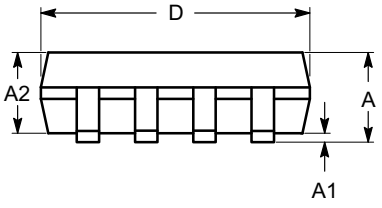
PACKAGE DIMENSIONS

TSSOP8, 4.4x3
CASE 948AL−01
ISSUE O

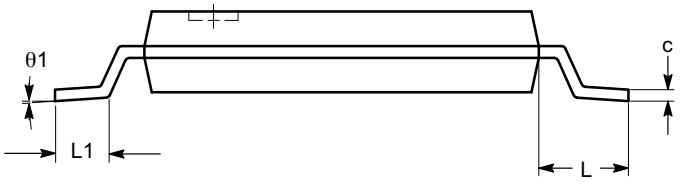


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
θ	0º		8º



SIDE VIEW



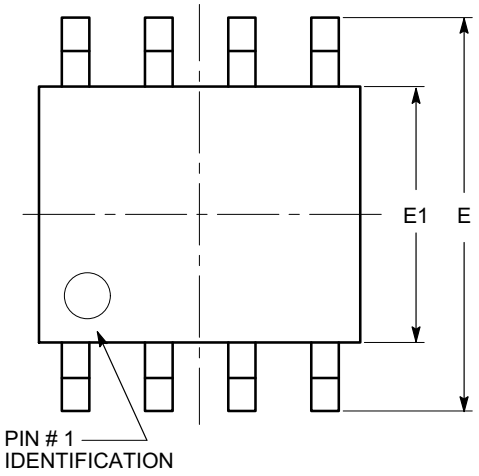
END VIEW

Notes:

(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

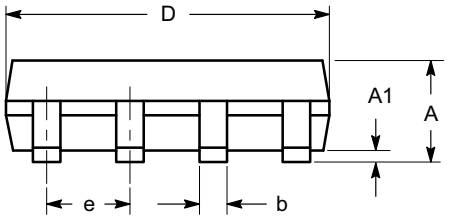
PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD−01
ISSUE O

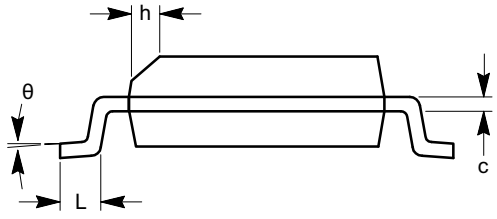


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0º		8º



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

Table 6. ORDERING INFORMATION

Part Number	Marking	Package Type	Temperature
P2040BF−08−ST	P2040BF	8−Pin SOIC, Tube, Pb Free	Commercial
P2040BF−08−SR	P2040BF	8−Pin SOIC, Tape and Reel, Pb Free	Commercial
P2040BG−08−ST	P2040BG	8−Pin SOIC, Tube, Green	Commercial
P2040BG−08−SR	P2040BG	8−Pin SOIC, Tape and Reel, Green	Commercial
P2040BF−08−TT	P2040BF	8−Pin TSSOP, Tube, Pb Free	Commercial
P2040BF−08−TR	P2040BF	8−Pin TSSOP, Tape and Reel, Pb Free	Commercial
P2040BG−08−TT	P2040BG	8−Pin TSSOP, Tube, Green	Commercial
P2040BG−08−TR	P2040BG	8−Pin TSSOP, Tape and Reel, Green	Commercial
I2040BF−08−TT	I2040BF	8−Pin TSSOP, Tube, Pb Free	Industrial
I2040BF−08−TR	I2040BF	8−Pin TSSOP, Tape and Reel, Pb Free	Industrial
I2040BG−08−TT	I2040BG	8−Pin TSSOP, Tube, Green	Industrial
I2040BG−08−TR	I2040BG	8−Pin TSSOP, Tape and Reel, Green	Industrial
I2040BF−08−ST	I2040BF	8−Pin SOIC, Tube, Pb Free	Industrial
I2040BF−08−SR	I2040BF	8−Pin SOIC, Tape and Reel, Pb Free	Industrial
I2040BG−08−ST	I2040BG	8−Pin SOIC, Tube, Green	Industrial
I2040BG−08−SR	I2040BG	8−Pin SOIC, Tape and Reel, Green	Industrial

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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P2040B/D